Filing Date: March 24, 2004

Group Art Unit: 2030

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(Use several sheets if necessary)

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FORM (449* INFORMATION DISCLOSURE STATEMENT IN AN APPLICATION	Docket Number: 50019.273US01/P05808	Application Number: 10/808,635
	Applicant: Siew Siong Teo	

**U.S. PATENT DOCUMENTS EXAMINER** DOCUMENT NO. DATE NAME **CLASS SUBCLASS FILING DATE** IF APPROPRIATE INITIAL TLE 6,075,354 6/13/00 Smith et al. 323 313 TLE 2/6/01 374 US 6,183,131 B1 Holloway et al. 172 TLE US 6,232,828 B1 Smith et al. 327 539 FOREIGN PATENT DOCUMENTS DOCUMENT NO. DATE COUNTRY **CLASS SUBCLASS** TRANSLATION YES NO OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.) TLE Randall L. Geiger et al., "VLSI Design Techniques for Analog and Digital Circuits," 1990 (2 pages) (p 369) TLE Phillip E. Allen et al., "CMOS Analog Circuit Design," 1987 (3-pages) (pp 591 and 595)

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EXAMINER /Terry Englund/ DATE CONSIDERED 09/06/2006

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